Static and Dynamic Stability Criteria of 6T SRAM Bit Cell

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***Abstract*—The consolidated 6T SRAM bit cell is comprised of six MOS transistors, four of which pertain to the individual inverter loop structure for every single bit of data to be accessed. Such bit cells operate with intrinsic nonlinear properties, as predicted by the MOSFET behavior. It is of deep interest that the well functioning of the overall memory structure is guaranteed, given that the stability of individual cells is studied further beyond the elementary for both their static and dynamic criteria. We intend to present an overview of fruitful knowledge around the noise margins associated to the inverter loop, backed by simulations performed in Synopsis HSPICE with a 45-nm CMOS model. The information envisioned through these simulations may be useful futurely to improve a bit cell's overall operation.**

I. Introduction

A circuit composed of two back-to-back connected inverters (Fig. 1), namely distinguished in feedback and feedforward, can be simulated for its DC solution. Equivalent to such topology is the 6T SRAM bit cell (Fig. 5), which counts with three DC solutions: a pair of stable ones, in direct correlation to the binary values, and a metastable solution, commonly defined as the saddle point [1]. All are coincident to the only points where voltage transfer curves (VTC) of both feedback and feedforward inverters intertwine, drawing what's referred to as the "butterfly curve". Would a noise source to be introduced, i.e., a DC voltage source V_n, there should be a margin of adverse voltage branched in the circuit to which the cell would hold its stability of input and output logic values without flipping to an alternate state, hence the definition of the Static Noise Margin (SNM).

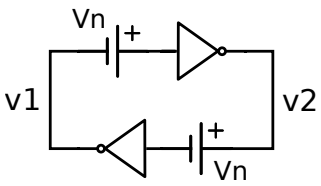

Fig. 1. Closed-loop configuration of two back-to-back connected inverters.

The data stability notion of SNM, alongside with probabilistics, presents itself as useful enough for designing of the memory in many cases, but disregards that the cell operates in a dynamic environment, thus limiting the handling of stability information to a short and barely flexible concept. Attempts at grasping the transient behavior of the cell through simulations have proved valuable to a future interest of better dimensioning and perfecting desired aspects of the cell's performance.

II. Static Noise Margin

The static condition to a stable inverter loop bit cell requires it to hold on to its state at both input and output, for any DC voltage adversely applied to it, under a certain margin. The butterfly curve, as previously mentioned, results from the intercepting of the feedback and feedforward inverter's voltage transfer curves, such as in Fig. 2.

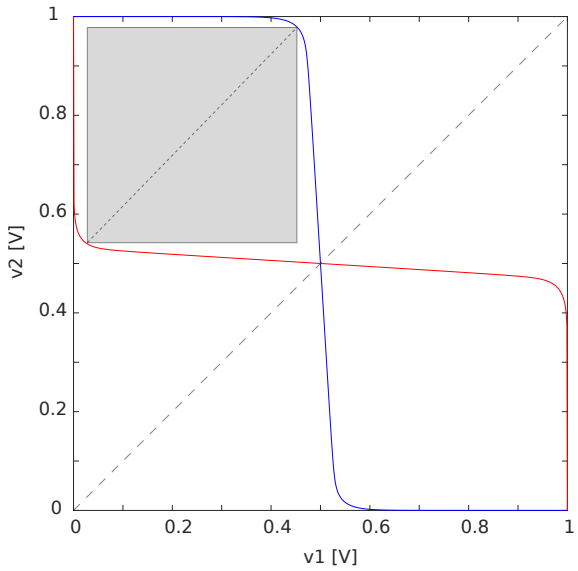

Fig. 2. Butterfly curve, derived from the intercepting of the inverters' VTC, and the largest possible square enclosed by one of its lobes.

A useful technique for obtaining the numeric value of the SNM is to search for the largest possible square enclosed by the individual lobes of the butterfly curve [2]. Alternatively, the square's diagonal is also meaningful - if the plot were to be rotated and aligned to the quadrant's bisector axis, depicted as the larger dashed line in Fig. 2, then the diagonal (i.e., the smaller dashed line) would match the distance between the maximum and minimum values of the rotated feedforward

and feedback VTC, as depicted in Figs. 3 and 4. Finally, a square geometry with this given diagonal ensures the SNM by the division of the measurement by $\sqrt{2}$, which implies the square's own dimension:

$$SNM_1 = \frac{|(\max(VTC_1) - \min(VTC_2))|}{\sqrt{2}} \quad (1)$$

$$SNM_2 = \frac{|(\min(VTC_1) - \max(VTC_2))|}{\sqrt{2}} \quad (2)$$

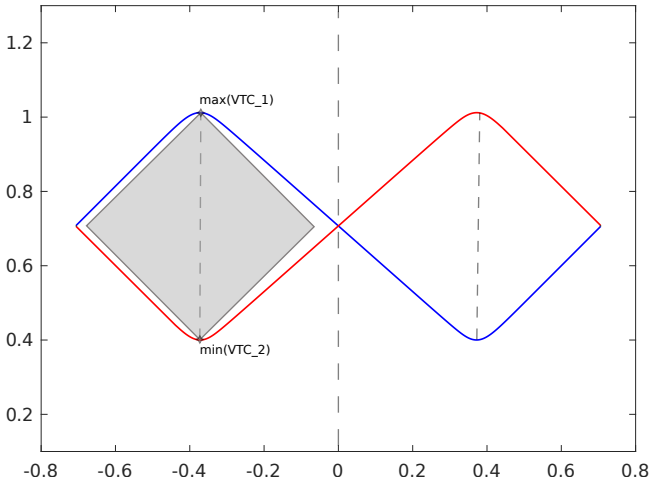

Fig. 3. Rotation of the butterfly curve in vertical alignment to the bisector axis.

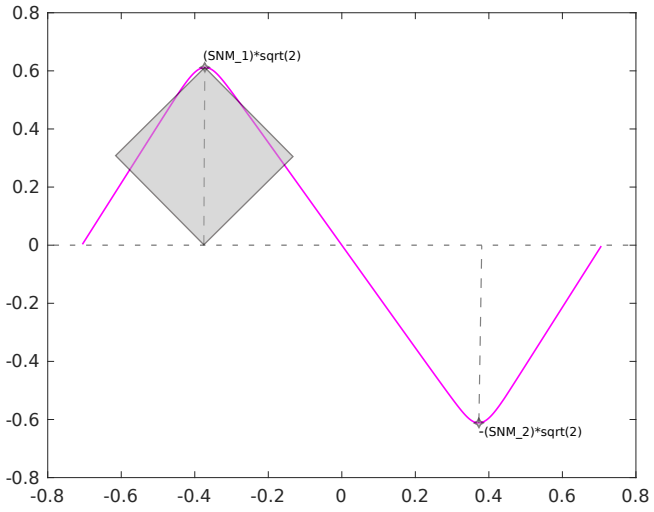

Fig. 4. Subtraction of VTC_1 by VTC_2, capturing maximum and minimum values of the resulting curve in accordance to the squares' diagonal lengths.

The introduced butterfly curve was drawn by simulating for the open-loop of a single one of the identical inverters and intercepting it with its duplicate. The PMOS and NMOS widths chosen for the device are of $313,28nm$ and $200nm$, respectively, which allow for a more symmetric curve when composing the closed-loop configuration, for demonstration purposes.

One could argue that the "actual" butterfly curve, regarding both inverters simultaneously, would differ to that of a single open-loop inverter with the same PMOS and NMOS dimensions, transcribed to the matching closed-loop by the aforementioned intercepting of the transfer curves. Further simulations prove otherwise: the SNM maintains its value either way. Therefore, the butterfly curve and the SNM can be assured solely on the open-loop characteristics of isolated inverter components, whether components of a symmetric loop or not. As such, asymmetric loops, pairs of inverters with different MOS dimensions, will require the open-loop transfer curves to be distinguished between feedback and feedforward inverters, aiming to correctly compose the resulting butterfly curve.

III. Dynamic Noise Margin

As previously mentioned, knowledge of the static criteria to data stability might not suffice. The SRAM operates in a dynamic environment, as do the individual bit cells. The concept of a sufficient adverse voltage to flip the bit isn't substantial enough because noise interferes with the circuit performance over time, and the period of time the noise is active at any given read/write access has a strong influence on whether it will go back to its original state or flip to an opposite state.

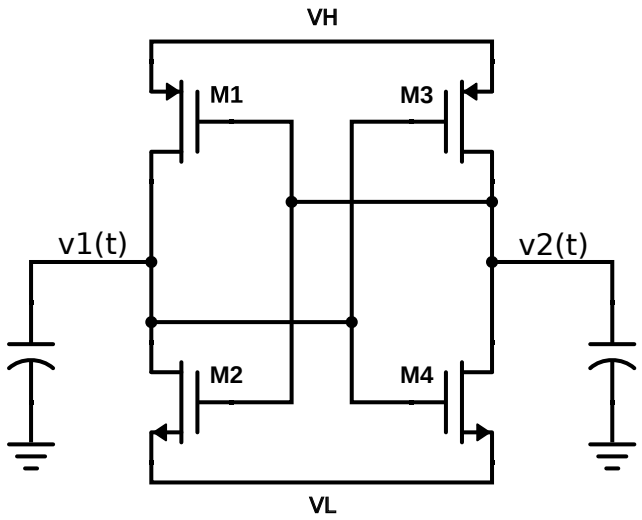

Fig. 5. Non-accessed 6T Static Random Access Memory bit cell.

The 6T SRAM bit cell, presented in Fig. 5, is regarded as non-accessed when it's not undergoing any read/write operation. In this case, the circuit input and output, $v_1(t)$ and $v_2(t)$, respectively, can be thought of as the voltage drop to discrete capacitor elements, taking into account the memory bit-line parasitic capacitance. Under regular circumstances of reading or writing of the memory, the remaining pair of NMOS transistors would be driven to a logic '1' by the word-line.

A. *Dynamic behavior to external noise sources*

Simulations were performed by introducing a draining current noise source of $53,3\mu A$ to the cell's input and verifying its dynamics for both different pulses and MOSFET dimensions. Such parameters interfere with how the cell will respond under transient exposure. In Fig. 6, the current pulse selected is of $3ns$, with all two PMOS and two NMOS device widths ranging from $100nm$ to $500nm$.

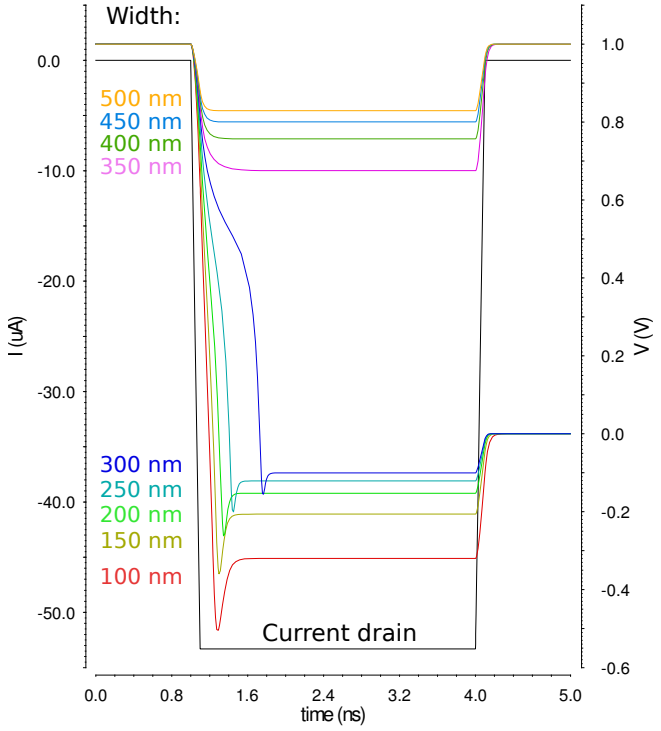

Fig. 6. Dynamics of the SRAM bit cell for a draining current applied to the input of the inverter loop.

Clearly, at some critical value between $300nm$ and $350nm$, the cell destabilizes and alternates its state from logic '1' to '0'. For any scenario where it biases towards the same equilibrium of stability after the current pulse is applied, it can be said that the cell did not leave its initial region of convergence, whereas, in the opposite case, the cell has fallen onto the opposite domain of attraction, due to the other stable solution.

The larger the MOSFET width, the longer will be the noise in the input to which the cell will still hold the bit of data, i.e., return to its original state equilibrium, besides the noise applied to it. Whether the logic value flips or not, the behavior is represented over time by singular trajectories on the space state (Fig. 7), and the system dynamics is distinguished by how fast it tends to accomodate between each disturbance.

Analysis of the cell's response when subjected to a limited external noise attests that it does operate under the influence of attracting convergence points, but is not sufficient to clarify it and better characterize the space state for a non-accessed bit cell, as would do a two-dimensional vector field, for instance. The following section pursues a better understanding of the regions of convergence, generalizing trajectories on the space state by simulating for multiple initial conditions of input and output voltage values.

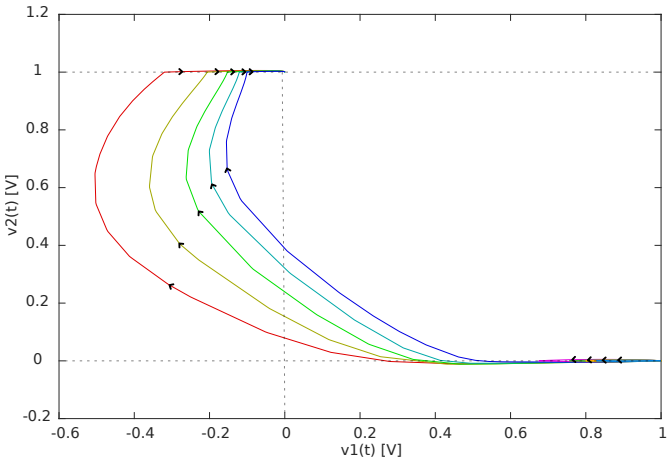

Fig. 7. Trajectories on the space state, associated to each circumstance of the cell's behavior when subjected to noise for a time period.

B. *Dynamic behavior to gridded initial conditions*

Primarily, these SPICE simulations focused on close observation to the 6T bit cell's nonlinear dynamics, subjected to a grid of initial conditions on the space state. Trajectories were then associated to each point on the grid as the cell biased towards one of its three DC solutions, and data manipulated as to approximate the space state to an approachable vector field. Every trajectory on the grid of Fig. 8 is composed of 5000 samples, spaced consecutively by a time interval of $1ps$. For better resolution of distinguishable trajectories, the samples were greatly narrowed.

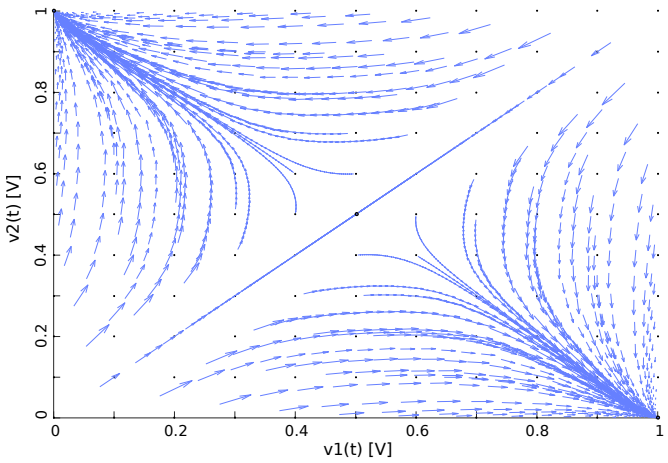

Fig. 8. Trajectories on the space state for an 11x11 grid of initial conditions, over $5ns$ transient simulations.

The space state to an inverter loop circuit is segmented into two regions of convergence, as verified for a noise source

introduced in the system, either flipping the cell or unbalancing it until the return to an initial state [3]. If initial conditions (IC) of input and output values were set beforehand, in place of an external noise, the dynamics of the cell would similarly converge to the circumstances of stability.

Simulating for an IC grid on the space state meets these expectations, as different starting points reenact trajectories of attraction towards the pair of stable conditions and, possibly, the metastable equilibrium, which draws the separatrix between the other two domains [4]. Based on a set of trajectories that roughly summarize the non-accessed cell dynamics, methods of two-dimensional interpolation allow for an extended perception of the plane as a vector field, as demonstrated in Fig. 9.

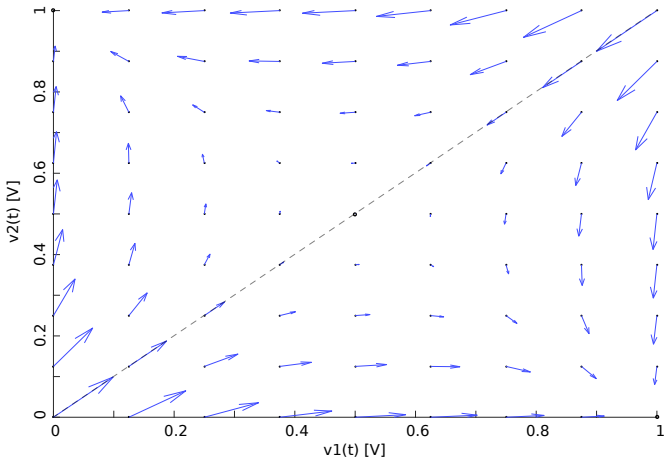

Fig. 9. Bit cell's space state dynamics in light of a vector field, given a 9x9 grid of initial conditions.

The significance of the individual trajectories and each vector quantity that composes it lies on the understanding that, for every uniform sample period, according to the space state condition, the cell may be more or less inclined to converge to a stable equilibrium. The vector field, as such, comprises the information of direction and velocity to different points on the grid. In other words, if each vector $\vec{A}$ were to be thought in terms of its components, then the projection of it on the input axis is a measurement of horizontal velocity (A_{v1}) and, similarly, the projection on the output axis ensures the up or downwards velocity (A_{v2}). As a whole, these quantities compose the space state vector field given by Equation (3):

$$\vec{A}(v1(t), v2(t)) = A_{v1}(t)\vec{i} + A_{v2}(t)\vec{j} \tag{3}$$

For every point on the plane, the cell follows a pattern, until stabilizing on either one of the DC solutions. The observable velocity vectors obtained in the transient simulations for the initial conditions underlie how fast the non-accessed cell converges to said equilibrium states. A better analogy can then be computed as the divergence of the vector field, illustrated by a three-dimensional coloured mesh in Fig. 10, where the lower divergence implies a convergence point, and can be expressed mathematically in terms of the vector field $\vec{A}$ (4).

$$\nabla.\vec{A}(v1, v2) = \frac{\partial A_{v1}}{\partial v1} + \frac{\partial A_{v2}}{\partial v2} \tag{4}$$

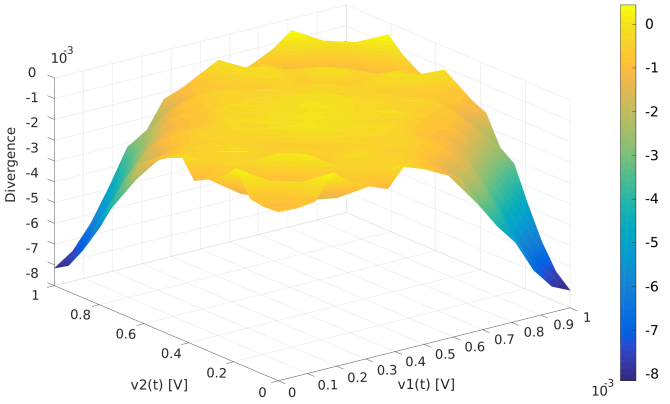

Fig. 10. Divergence of the space state vector field for the non-accessed 6T SRAM bit cell.

Despite limited resolution to the mesh interpolation of the vector field and subsequent divergence computation, this further notion of the space state contemplates the two converging points, or bi-stable solutions, visualized as the blue lateral fringes, while the meta-stable equilibrium is of a nearly neutral stance, hence why it's commonly referred to as the saddle point.

IV. Conclusion

The stability of a memory cell plays a major role on its performance, whether on standby, aiming to retain data, or submitted to non-destructive read and successful write operations [4].

We surmised the most prominent techniques and information regarding the static and dynamic criteria for the state-of-the-art 6T SRAM bit cell, providing further approaches to the non-accessed behavior under theoretical situations of distress. The analysis of the space state as a vector field conceives the relevant notion of its divergence, allowing for future purposes of enhancing the cell's dynamics. Studies to come may further explore the pertinence of some of the memory's characteristics in relationship to the introduced conceptions.

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